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Prioritized state-dependent buffer-management schemes in ATM switch

ABSTRACT

This paper presents a buffer management scheme using two different service disciplines to improve the quality of service among traffic classes. The results obtained in experiments show the effectiveness of proposed method for both modelled traffic and real network trace data.

INTRODUCTION

The architecture and the performance of ATM switch have been an area of intensive research and development since the adoption of ATM as the underlying technology for Broadband ISDN, provides a common, flexible and theoretically simple solution for the transmission, multiplexing and switching of all telecommunication services. In order to accommodate such a diverse set of requirements ATM can only offer some form of compromise. Therefore, it is not an ideal solution for any individual application, but gives a reasonable service for a wide variety of requirements.

ATM has two types of service categories: the *Guaranteed Type* (GT) and the *Best Effort Type* (ET). Best effort is suitable for data communication because it is not delay sensitive. The best effort category has two service classes: *Unspecified Bit Rate* (UBR) and *Available Bit Rate* (ABR). The guaranteed type of ATM traffic consist of *Variable Bit Rate* (VBR) as well as the *Constant Bit Rate* (CBR). The guaranteed category is suitable for real time multimedia services as video, voice and real time data [1]

For each service, particular techniques have to be employed in order to maximize the network efficiency and to deliver the required Quality of Service to the end users. Techniques such as *Fast Reservation Protocol* [2] offer some measure of statistical gain for little extra switch implementation cost. However, greater network efficiency can be achieved for high peak bitrate bursty traffic by dynamic resource allocation.

This paper proposes a new priority scheme for the scheduling of an output-buffered ATM switch. The rest of the paper is organized as follows. In Section 2, the proposed buffer management scheme and the priority service discipline are discussed. Section 3 gives a detailed description of implementation of the neural server unit. In Section 4, discussion of simulation results is provided. Section 5 concludes with a summary of the paper.

BUFFER MANAGEMENT SCHEME

An N x N ATM switch with output buffers is considered in this section as shown in Figure 1. Each output port has a buffer where cells arrive in batches. Let the buffer size of each output port be B. As mentioned above, two types of service categories are discussed in examination - the GT and the ET. It is clear that each service type has it own requirements on delay and cell loss rate.

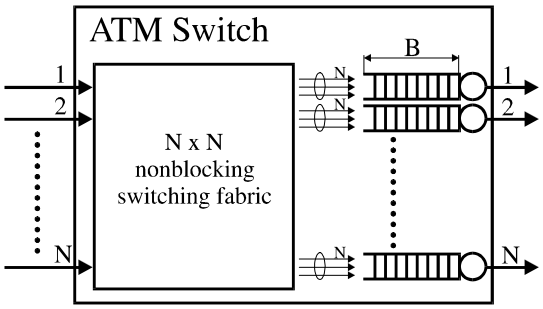

Figure 1. ATM switch with output buffers

To reduce the cell loss rate for ET class as well as delay for GT class, we propose a buffer management scheme as shown in Figure 2.

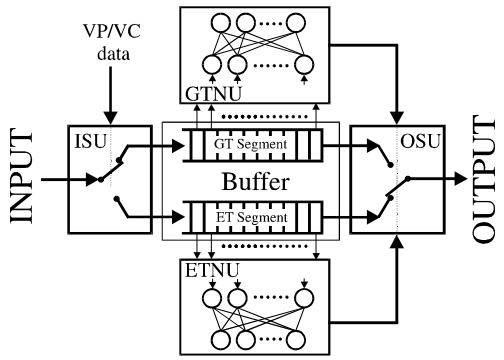

Figure 2. Buffer management scheme

The arriving ET cells are placed into ET Segment of the buffer, while the arriving GT cells are placed into GT Segment of the buffer. Both ET and GT segments serve the cells according to the FIFO discipline, thus the buffer can be implemented by simple shift register. The states of both ET and GT segments are examined by the *Best Effort Traffic Neural Unit* (ETNU) and *Guaranteed Parameters Traffic Neural Unit* (GTNU) respectively. These units control directly *Output Switching Unit* (OSU in Fig.2) which in each time slot compares the levels of both inputs and sent the cell from the appropriate segment of the buffer (ET or GT) to the output line.

Two pointers, namely the ET pointer and the GT pointer, are associated with the position of the latest arrived ET and GT cells, respectively. When the buffer is full, the two pointers are next to each other. Under such circumstances, any GT arrival is discarded, but ET arrival will be stored by replacing a GT cell in the buffer. For the memory allocation scheme between both ET segment and GT segment, we propose a *Partially Shared Model* (PSM) [4]. In the PSM, each queue may use free memory but only up to a fixed level. Appropriate minimal length of ET Segment and length of GT Segment are fixed to be B^{ET}_{min} and B^{GT}_{min} respectively. For 16 x 16 ATM switch studied in this paper, a 2048-location total buffer capacity *B* was found to produce a good compromise between CLR as QoS parameter and the ability of neural units (ETNU and GTNU) to control queues.

Both ETNU and GTNU are backpropagation neural networks and may be separately trained. This performance significantly decreases training time. In simulation experiments several neural networks were implemented using the California Scientific Software *BrainMaker*. In the beginning of the learning experiments, many different neural network architectures were investigated, ranging in complexity from single hidden layer network to more complex structures. However, by using networks with 2 hidden layers stable results were obtained. The example results are given below:

- For a ETNU with 128 neurons in the input layer, 12 neurons in the first hidden layer and single output neuron, the learning rate and momentum term were 0.2 and 0.6, respectively. After 6300 lessons, all states of controlled zone of ET queue were classified accurately. The learning process took about 2 hours using the accelerator.
- A set of 64 x 6 x 1 neurons (GTNU) was trained during 3000 lessons. It took about 1 hour on the accelerator.

In the training phase both neural networks were prepared to calculate some cost function C^{xx} of storage particular cell in GT or ET segment of buffer. We define

$$C^{XX} = C_D^{XX} + C_C^{XX} \qquad (1)$$

where *XX* is the segment index (ET or GT) and $C^{xx}{}_D$ and $C^{xx}{}_C$ are delay and "capacitance" components of the cost function C^{xx} respectively.

We assume that $C^{xx}{}_D$ is some function of mean delay $\underline{t}_{xx}$ of cells stored in controlled zone of XX segment of the buffer. Thus, $C^{xx}{}_D$ may be written as

$$C_D^{XX} = f(\underline{t}_{xx}), \text{ where } \underline{t}_{xx} = \frac{\sum_{i=1}^{n_{XX}} t_i}{n_{XX}} \qquad (2)$$

In our proposition

$$C_D^{GT}(t) = C_D^{ET}(t + \Delta t) \text{ and } 0 \le C_D^{XX} \le 0.5 \qquad (3)$$

For capacitance component of C^{XX} we define

$$C_C^{XX} = \frac{n_{XX}}{2B_{\min}^{XX}} \qquad (4)$$

where n_{xx} is number of cells stored in controlled zone of XX segment of the buffer.

Because $n_{XX} \le B^{XX}{}_{min}$, we have $C^{xx}{}_C \le 0.5$ and finally, according to (3) and (4):

$$0 \le C^{xx} \le 1 \qquad (5)$$

As mentioned earlier, in training phase the neural networks of both GTNU and ETNU control units are prepared to calculate C^{GT} and C^{ET} functions

respectively. As depicted in Figure 2, the output signals of both control units are compared in OSU. OSU connect the output line to this segment of the buffer which is pointed by greater level of their control signal.

This idea is inspired by Little's formula, which states that average number of customers in a ergodic queueing system is equal to the average arrival rate of customers to that system, times the average time spent in that system, thus proposed comparation of the cost functions is a good criterion to decide the service order in a queueing system described in this paper.

SIMULATION EXPERIMENTS

In this section, we examine the performance of an output-buffered ATM switch using proposed priority scheme. In the experiments, we assumed that the capacity of memory buffer is fixed at 2^{10} = 1024 cells. The neural controlled zones of both GT and ET queues are fixed at $B^{GT}_{min} = 64$ and $B^{ET}_{min} = 128$ cell locations respectively.

The performances of the proposed queuing architecture are checked in terms of the *Mean Cell Transfer Delay* (MTD) and *Cell Loss Ratio* (CLR) among the classes of the traffic. In the experimental studies followed it was assumed that the input cell process constituted a *Bernoulli Batch Process* (BBP) - all cells arrive at the beginning of a time slot with the same probability. We assume throughout, that destination output addresses of the cells are uniformly distributed with probability 1/N that a given output of switch is chosen. This means that the maximal number of cells which may arrive to the queue in a given time slot is equal to N. Note that the bit rate in the output line is assumed to be 136 Mbps which is the standard value available for ATM payload in the 155 Mbps stream.

Average delay time (MTD) for GT class is significantly smaller that in the SPS, while MTD for ET traffic is larger than that in the SPS. Thus, the improvement of the delay time for GT class of traffic is at the expense of the delay time for the ET traffic.

Figure 3 gives the MTD versus probability p_{GT} that an incoming cell is a delay-sensitive one. The arrival rate ρ in this case is constant (ρ = 0.7).

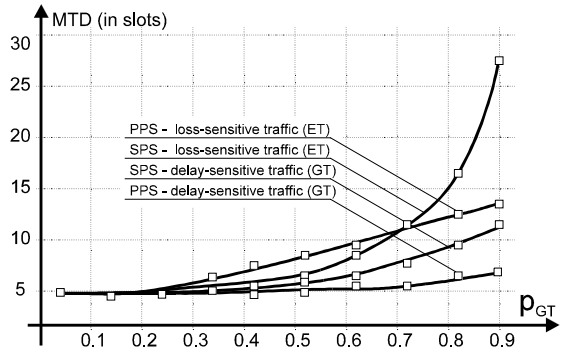

Figure 3. MTD versus probability p_{GT}

Figure 4 illustrates that in SPS the MTD of GT traffic changes slowly and MTD of ET cells increases quickly.

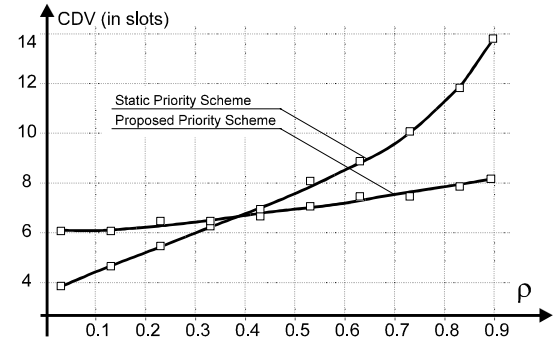

Figure 4. Cell Delay Variation vs. offered load

In the proposed priority scheme, the MTD of each class changes very slowly. Figure 4 confirms that the variance of MTD in proposed priority scheme is smaller than that in the SPS.

The cell loss rate of loss-sensitive class of traffic (ET) in proposed priority scheme is significantly smaller too than that without priority scheme as well as Static Priority Scheme.

In the following, bursty arrival [6] will be considered to discuss the influence of traffic burstiness on both schemes compared in the paper. In next experiment we compare the cases with and without use priority control in the ATM switching system. In this case the 95% - percentile cell delay vs. the number of the traffic sources is considered. In this experiment, the background CBR traffic ρ_b = 0.4 has been used to obtain a close reality experiment environment. The traffic under test consists of a number of MPEG2/2 Mbps streams. The data used in the experiments was collected from the files available by Internet which consist in each case of not more than 2 MB coded videos. About 32 MB data were proceeded by software to

obtain a form appropriate for use in the experiments.

The use of PPS significantly improved the system parameters by appropriately ordering the cells from different classes of traffic. When the buffering system tested does not use any ordering method, the CAC function may accept about 25 new MPEG traffic sources. In contrast, PPS usage permit connection of 10 sources more. In this case, the load offered to the system is near the theoretical border of the output line capacity. The same effect may be observed in next experiment. In this case, the background traffic has been obtained by working ATM network called *VISTAnet* which is a gigabit testbed sponsored by the *National Science Foundation* and was designed to implement a medical imaging application and LAN-LAN services [7] over large distances in North Carolina. The files used as a bursty traffic source in simulation experiments are available by *anonymous ftp from kira.mcnc.org under pub/vista.net*. The bursty background load at mean rate $r_b = 0.5$ and the VBR character, was used to examine PPS properties in the case when the number of CBR 64 kbps sources are connected to the switch under study.

In the case without PPS usage, only 700 CBR sources may be connected to the system. The PPS usage permit to increase the number of CBR sources in the system.

CONCLUSIONS AND SUMMARY

In this paper, a buffer management scheme for ATM switch with two different classes of traffic which require different QoS is proposed. The priority discipline with neural control is studied in the scheduling of an output buffered ATM switch. The concept of discussed priority scheme is inspired from Little's formula, and it provides a good cost criterion for the decision of service order in ATM networks. This proposed priority scheme considers the relative number of cells in the queue for each class of traffic as well as mean cell delay to decide the service order. The result of the simulation experiments shows that when most of the traffic is ET, the average delay time for this class decreases negligibly, but the average delay time for GT traffic increases slightly. Therefore, it is less beneficial to employ state-dependent priority schemes when most of traffic is ET. However, when most traffic is GT, the average delay for GT class decreases a lot, at the expense that the average delay time of GT class increases slightly. Thus, it is beneficial to use proposed in the paper priority scheme when most traffic is GT.

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